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REMARKS

The following remarks are made in response to the Non-Final Office Action mailed April 5, 2006. Claims 1-38 were rejected. With this Response, claims 1-3, 8, 10, 12, 18, 25, and 26 were amended. Claims 1-38 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 112

Claims 1-3, 8, 10, 12, 18, 25, and 26 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 1-3, 8, 10, 12, 18, 25, and 26 have been amended to recite **a column address strobe latency select signal**. The column address strobe latency select signal is described in the specification beginning on page 7, line 28 which states "CAS latency one select (CL1) line 142 is electrically coupled to bypass 114 and multiplexer 122. Signal CL1 is true if a CAS latency of one is selected. CL1 is false if a CAS latency greater than one is selected." The column address strobe latency select signal is applied on path 142 in Figures 3 and 4.

In view of the above, Applicant respectfully submits that the above rejection of claims 1-3, 8, 10, 12, 18, 25, and 26 under 35 U.S.C. § 112 should be withdrawn. Allowance of claims 1-3, 8, 10, 12, 18, 25, and 26 is respectfully requested.

Claim Rejections under 35 U.S.C. § 102

Claims 1-3, 17, 18, and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Usami, U.S. Patent No. 6,205,516 ("Usami").

Applicant submits that Usami fails to teach or suggest the invention recited by independent claim 1 including **a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a

command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - Col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - Col. 10, line 1).

The Examiner submits "SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3." (Office Action, page 4). Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in independent claim 1. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal.

In view of the above, Applicant respectfully submits that the above rejection of claim 1 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 2 and 3 further define patentably distinct independent claim 1. Accordingly, Applicant believes these dependent claims are also allowable over the cited reference. Allowance of claims 1-3 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Usami fails to teach or suggest the invention recited by independent claim 17 including **a bypass circuit that bypasses the first in/first out memory; and a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first**

out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.

In view of the above, Applicant respectfully submits that the above rejection of claim 17 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claim 18 further defines patentably distinct independent claim 17. Accordingly, Applicant believes this dependent claim is also allowable over the cited reference. Allowance of claims 17 and 18 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Usami fails to teach or suggest the invention recited by independent claim 31 including **means for receiving the data read from the array of memory cells to bypass the means for storing data; means for retrieving the data from the means for storing the data if column address strobe latency is greater than one; means for retrieving the data from the means for receiving the data if the column address strobe latency is one.**

In view of the above, Applicant respectfully submits that the above rejection of claim 31 under 35 U.S.C. § 102(b) should be withdrawn. Allowance of claim 31 is respectfully requested.

Claim Rejections under 35 U.S.C. § 103

Claims 4-16, 19-30, and 32-38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Usami.

Dependent claims 4-16, 19-24, and 32-38 further define patentably distinct independent claim 1, 17, or 31. Accordingly, Applicant believes these dependent claims are also allowable over the cited reference.

For the same reasons as discussed above with reference to claim 1, Usami fails to teach or suggest the invention recited by independent claim 25 including **a bypass circuit configured to bypass the memory circuit; a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal; a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.**

In view of the above, Applicant respectfully submits that the above rejection of claim 25 under 35 U.S.C. § 103(a) should be withdrawn. Dependent claims 26-30 further define patentably distinct independent claim 25. Accordingly, Applicant submits that these dependent claims are also allowable over the cited reference.

In addition, in regard to claims 4-11, 19-21, 25-30, and 33-38 the Examiner has taken official notice that any combination of clock edges can be combined to provide the instruction to receive data. (Office Action, page 5). As indicated in the Manual of Patent Examining Procedure, however, "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." M.P.E.P. § 2144.03(A). "It would not be appropriate for the Examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well known." *Id.* (Emphasis in original). Applicant contends that the further limitations recited in these claims are not well-known facts that are capable of instant and unquestionable demonstration as being well-known. Accordingly, Applicant respectfully requests allowance of these claims, or requests pursuant to M.P.E.P. § 2144.03 that the Examiner cite a reference to teach the further limitations of claims 4-11, 19-21, 25-30, and 33-38.

Further, in regard to claims 12-16, 22-24, and 32, the Examiner admits that Usami fails to disclose a tri-state output (claims 12 and 24), a first in/first out memory (claims 13 and 32), a low power synchronous dynamic random access memory (claim 14), a double data rate-I synchronous dynamic random access memory (claim 15), a double data rate-II synchronous dynamic random access memory (claim 16), a data delay circuit (claim 22), and an off chip driver (claim 23). (Office Action, page 5). The Examiner states that it would have been obvious for a person of ordinary skill in the art to combine these limitations with the random access memory of Usami. (Office Action, page 6).

Since the Examiner has not cited any reference to teach the further limitations of claims 12-16, 22-24, and 32 it appears that the Examiner is taking official notice. Applicant contends that the further limitations of claims 12-16, 22-24, and 32 are not well known facts that are capable of instant and unquestionable demonstration as being well known. Applicant respectfully requests allowance of these claims, or requests pursuant to M.P.E.P. § 2144.03

that the Examiner cite a reference to teach the further limitations of claims 12-16, 22-24, and 32.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-38 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-38 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark A. Peterson at Telephone No. (612) 573-0120, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 5th day of July, 2006.

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